REMARKS

In accordance with the foregoing, claims 1, 10, 17-18, and 22-29 are amended. No new matter is presented in any of the foregoing and, accordingly, approval and entry of the amended claims are respectfully requested. Claims 1-29 are pending and under consideration.

While block 2b of the Office Action Summary indicates that the Action is non-final, item 52 on page 34 of the current Action indicates that "THIS ACTION IS MADE FINAL." As confirmed in a telephone conversation between the Examiner and the Applicant's representative of July 11, 2005, the Examiner confirmed that the current Action is a non-final Action, and is so reflected in the USPTO file history.

ITEMS 3-4: OBJECTION TO CLAIMS 18 AND 23

In items 3 and 4, the Examiner objects to claims 18 and 23 because of informalities. (Action at page 2).

Claims 18 and 23 are amended as suggested by the Examiner, and Applicants request the objections be withdrawn.

ITEM 6: REJECTION OF CLAIM 23 UNDER 35 U.S.C. 112, SECOND PARAGRAPH

In item 6, the Examiner rejects claim 23 under 35 U.S.C. 112, second paragraph as being indefinite. Applicants submit that claim 23, as amended herein, complies with 35 U.S.C. 112, second paragraph and request the rejection be withdrawn.

TRAVERSE OF 35 U.S.C. §102(b) AND 35 U.S.C. §103(a) REJECTIONS

The Examiner rejects claims 1-6 and 8 under 35 U.S.C. §102(b) as anticipated by Parady (U.S.P. 5,933,627); rejects claims 1-2, 8-9, 17, 23, 25, 28, and 29 under 35 U.S.C. §102(b) as anticipated by Fernando et al. (U.S.P. 6,272,616), rejects claims 7 and 9 under 35 U.S.C. §103(a) as being unpatentable over Parady in view of combinations of Dowling (U.S.P. 6,170,051) and Fernando, and rejects claims 10-16, 18-22, 24, and 26-27 under 35 U.S.C. §103(a) as being unpatentable over Fernando in view of combinations of Parady and Dowling.

The rejections are traversed.

Independent claims 1, and 24-27, (all as amended) recite, respectively, a processor control apparatus and a processor, using claim 1 as an example, including "a plurality of instruction control units issuing a series of instructions to said plurality of arithmetic units, wherein at least one of said instruction control units switches between a first execution process driving said plurality of arithmetic units by a single series of instructions issued from a single one of the plurality of instruction control units and the plurality of arithmetic units execute the single

series of instructions concurrently both upon the single series of instruction including different commands for each of the plurality of instruction control units and the single series of instructions including a same command for each of the plurality of instruction control units."

Independent claim 1, as amended, further recites an apparatus including "a second execution process correspondingly driving said plurality of arithmetic units by a plurality of different series of instructions issued respectively from more than one of said plurality of instruction control units and in which the processing by the plurality of arithmetic units can be synchronized." (Emphasis added).

Independent claim 10, as amended, recites a processor control apparatus, "wherein said plurality of series of instructions are issued to said plurality of arithmetic units from both a single one of the plurality of instruction memories and issued respectively from more than one of said plurality of instruction memories to enable said plurality of arithmetic units to be simultaneously and independently driven." (Emphasis added).

Independent claims 17-18, 22-23, and 29, all as amended, respectively recite a processor control apparatus, a processor, and a method, using claim 17 as an example, "wherein said plurality of series of instructions are issued to said plurality of arithmetic units from the instruction memory to be simultaneously and independently driven both upon the instructions including different commands for each of the plurality of instruction control units and including a same command for each of the plurality of instruction control units." (Emphasis added).

Independent claim 23 further recites " synchronously driving said plurality of arithmetic units."

Applicants submit that these features are not discussed by the art relied on by the Examiner, either alone or in an *arguendo* combination.

According to aspects of the present invention a processor, for example, controls a plurality of arithmetic units "wherein at least one of said instruction control units switches between:

(1) a first execution process driving said plurality of arithmetic units by a single series of instructions issued from a single one of the plurality of instruction control units and the plurality of arithmetic units execute the single series of instructions concurrently both upon

(1a) the single series of instruction including different commands for each of the plurality of instruction control units and

(1b) the single series of instructions including a same command for each of the plurality of instruction control units, and

(2) a second execution process correspondingly driving said plurality of arithmetic units by a plurality of different series of instructions issued respectively from more than one of said plurality of instruction control units and in which the processing by the plurality of arithmetic units can be synchronized." (Emphasis added).

Applicants submit that none of the art, alone or in combination, discuss or suggest, such a switching between a first execution process (1) and second execution process (2) where the first execution process also includes options for command sequences (1a) and (1b).

Further, in contrast to the art relied on by the Examiner, either alone or in combination, aspects of the present invention enable switching between simultaneously driving arithmetic units by issuing a single series of instructions (SIMD) from a instruction control unit and independently driving the arithmetic units by correspondingly issuing series of instructions (VLIW) from respective instruction control units connected with the arithmetic units.

Rather, Parady merely discusses handling blocked memory accesses of a program resulting from accesses to the memory that require waiting by switching between threads of the program. According to Parady, instructions are provided to an instruction buffer to be accessed by a dispatch unit (see, col. 3, lines 10-12) that includes an instruction cache and instruction buffers corresponding to a number of threads of the instruction. Thus, Parady discusses merely limitations to switchably executing portions or threads of a program responsive to an event.

Fernando merely discusses a digital processor alternatively operating in a single threaded mode, a single instruction mode and a multiple instruction mode that in response to a CFORK instruction, a control signal instructs a multiplexer to accept data from input line (36) from a fetch stage of a primary instruction pipeline, and a decoder in a secondary instruction pipeline is activated (see, col. 6, lines 40-50).

Dowling merely discusses very long instruction word (VLIW), a microprocessor design technology, and a chip capable of executing many operations within one clock cycle to reduce program instructions into basic operations that the processor can perform simultaneously.

Applicants submit that even an *arguendo* combination of any of the art relied on by the Examiner does not teach features recited by the independent claims, for example, of switching between a first execution process and second execution process where the first execution process also includes options for command sequences.

Rather, an *arguendo* combination of Parady in view of Dowling merely teaches switching between threads in response to a long-latency event, and an enhanced VLIW architecture. An

arguendo combination of Parady in view of Fernando merely teaches switching between threads in response to a long-latency event including a method to switch between a scalar command, an SIMD command, and an MIMD command. An *arguendo* combination of Fernando in view of Dowling merely teaches a method to switch between a scalar command, an SIMD command, and an MIMD command, and an enhanced VLIW architecture. An *arguendo* combination of Fernando in view of Parady merely teaches a method to switch between a scalar command, an SIMD command, and an MIMD command and switching between threads in response to a long-latency event.

Summary

Since features recited by the independent claims (and claims dependent thereon) are not discussed by the art relied on by the Examiner, either alone or in combination, the rejections should be withdrawn and claims 1-29 allowed.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: August 25, 2005

By: Paul W. Bobowiec

Paul W. Bobowiec
Registration No. 47,431

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501